The title of the article is Mixed Signal Neural Circuits for Shortest Path Computation

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The point of the article is circuital computation of a pathfinding neural network model.

The main idea of an article is to discuss the hardware realization of a recurrent spatiotemporal neural network for single source multiple-destination graphical shortest path problems.

The article contains three parts:

The first one is description of an used circuit. In this part, authors provide reader with necessary illustrations and detailed work description of the whole circuit and its elements. Circuit consists of 5 rows, each one contains four identical processing elements(PE). Each PE is made up of a 6-bit register, a D/A converter, a Comparator, a latch, and an AND gate. The D/A converter is a 6-bit, current mode D/A converter. It consists of six scaled current mirrors, with an integrating capacitor as load. Each current mirror can be turned on or off by a PMOS switch. By regulating the total currents that flow, the time for the capacitor to discharge to a certain level can be varied. Indeed, this is how the cost of a path is encoded. The 6-bit register holds the digital input to the D/A converter, hence its content determines the cost assigned to the PE.

Second part is dedicated for circuit implementation, i.e. description of circuit subsystems, such as D/A converter and Latch.

D/A converter consists of six scaled current mirrors. Since accurate current scaling is essential, cascode current mirrors are used instead of the basic mirrors. The currents are scaled from a maximum of 16 mA to a minimum of

16 mA/2J = 0.5 mA. Each current mirror is connected in series to a PMOS transistors, which acts as a switch. If the gate of the PMOS transistor is LOW, then current is allowed to flow; otherwise no current will flow in the current mirror.

The function of the latch is to produce a permanent HIGH output when the comparator output becomes HIGH. An inhibit signal is connected to all latches in the same row to make sure only a single latch activates. Also, the “start” input for all latches is used to initialize all the latches to low.

In the third part, authors provide reader with the simulation results.

Cost computation is done in terms of time taken by the D/A converter to discharge load capacitor from VDD to 2.5 V.

Authors provide a plot that shows the relationship between register content and the associated path cost. For each code, both the ideal time to fire and the actual time from circuit simulation are plotted.

All simulations are done through Hspice program. To ensure simulation result is as accurate as possible, the Hspice netlist is obtained directly from the extraction of actual circuit layout.

To conclude, authors summarize the work done, give examples of the application of the designed circuitry, confirm the correctness of its functioning, and determine the direction of further research.